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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,093	07/07/2003	Lars Erik Thon	AELU.P0006	8681

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EXAMINER	
LAM, TUAN THIEU	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 12/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/615,093	THON, LARS ERIK	
	Examiner	Art Unit	
	Tuan T. Lam	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitations of "generating a time delay in signals output from said multipliers, calibrating said delay element so as to match said time delay to a predetermined time period, summing time delayed signals to generate an equalized signal" of claim 21, "a plurality of multiplier circuits, coupled in series, for multiplying a signal in each of said multipliers, a plurality of delay elements for receiving said multipliers signals from said multipliers and for generating a time delay in said signal, said delay elements being coupled in series to sum said multiplied signal to generate an equalized signal, and a calibration circuit, coupled to said delay elements, for calibrating said delay elements so as to match said time delays to predetermined time periods" of claim 22 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: page 17, line 20-22, page 18, lines 1-2, page 18, lines 18, the following reference numbers 850, 860, 865, 870 and 840 are not shown in figure 13B, D0, D1, D2 and D3, transmission line 910 are not shown in figure 14.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing

should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: page 17, lines 4 and 16, "Figures 12A and B" are cited, however, there are no figures 12A and 12B. Did applicant mean 13A and 13B?

Appropriate correction is required.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, the recitation of "said multiplied signals" in line 7 lacks proper antecedent

basis.

In claim 11, the recitation of "said multiplied signals" in line 7 lacks proper antecedent basis.

In claim 21, the recitation of "generating a time delay in signals output from said multipliers" is indefinite because it is misdescriptive. Figures 5 and 6 shows the output signals from the multipliers (468, 470, 472, 474 of figure 5) is summed up by the summer 480. The recitation of "summing time delayed signals to generate an equalized signal" is indefinite because it is misdescriptive. The output of the multipliers are summed up by the summer 480 (figure 5). The time delay signals (outputs of 440, 450, 455 and 460) are not summed up by the summer 480. Clarification and correction are required.

In claim 22, the recitation of "a plurality of multiplier circuits, coupled in series, for multiplying a signal in each of said multipliers" is indefinite because it is misdescriptive. Figure 5 does not show the multipliers coupled in series. The recitation of "a plurality of delay elements for receiving said multipliers signals from said multipliers and for generating a time delay in said signal" is misdescriptive. The delay elements (440, 450, 455, 460 of figure 4) are coupled in series and are not receiving said multipliers signals. The recitation of "said delay elements being coupled in series to sum said multiplied signal to generate an equalized signal" is misdescriptive. The delay elements (440, 450, 455 and 460) delay the input signal. The delay elements do not sum the multiplied signals. Clarification and correction are required.

Claims 2-10 are indefinite because of the technical deficiencies of claims 1 and 11.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-7 and 11-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Shirani (US 2004/0193669).

Figure 1 shows a circuit comprising at least one delay element (LC circuits) for receiving a signal and for generating a time delay in said signal, calibration circuit (tuning circuit shown in figure 3), coupled to the delay element, for calibrating said delay element so as to match said time delay to a predetermined time period, and multiplier-summing circuit (18a-18n, 16a-16n and summing node) coupled to said delay element, for multiplying a signal output from said delay element and for summing said multiplied signal to generate and equalized signal as called for in claims 1 and 11.

Regarding claims 2, 4, 12 and 14, figure 3 shows the calibration circuit comprises a loop control (54, 56, 58) for receiving a reference signal (54), output from said delay element, and for generating a phase adjustment (output of the loop filter 58) based on said delay of said reference signal propagated through said delay element, and said delay element comprises selectable parameters (varactor diodes) for receiving a phase adjustment from said control loop for setting said selectable parameters based on said phase adjustment.

Regarding claims 3 and 13, figure 3 shows a phase detector and a loop filter.

Regarding claims 5 and 15, the transmission lines are seen as the inductors.

Regarding claims 6 and 16, the capacitance of the varactor diodes are adjustable.

Regarding claims 7 and 17, inductor and varactor diodes are lumped elements.

5. Claims 1-5, 9-15 and 19-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Roy et al. (US 2004/0131128).

Figure 4 shows a circuit comprising at least one delay element (delay elements 402, 404, 406) for receiving a signal and for generating a time delay in said signal, calibration circuit (tuning circuit shown in figure 5), coupled to the delay element, for calibrating said delay element so as to match said time delay to a predetermined time period, and multiplier-summing circuit (408, 410, 412, 414 and summing node) coupled to said delay element, for multiplying a signal output from said delay element and for summing said multiplied signal to generate and equalized signal as called for in claims 1 and 11.

Regarding claims 2, 4, 12 and 14, figure 5 shows the calibration circuit comprises a loop control (500) for receiving a reference signal (reference clock), output from said delay element, and for generating a phase adjustment (Vcntl) based on said delay of said reference signal propagated through said delay element, and said delay element comprises selectable parameters for receiving a phase adjustment from said control loop for setting said selectable parameters based on said phase adjustment.

Regarding claims 3 and 13, figure 3 shows a phase detector inherently having a loop filter.

Regarding claims 5 and 15, the transmission lines are seen as wires.

Regarding claims 9 and 19, said delay element comprises a plurality of stub transmission lines (parallel paths).

Regarding claims 10 and 20, said delay element further comprises a means for selecting (switches 703, 705, 707, 709) a length of said stub transmission lines to calibrate said delay element (each parallel path has different transmission line length).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 8 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shirani (US 2004/0193669) in view of Yu et al. (US 2003/0090339).

Figure 1 of Shirani shows a circuit comprising at least one delay element (LC circuits) for receiving a signal and for generating a time delay in said signal, calibration circuit (tuning circuit shown in figure 3), coupled to the delay element, for calibrating said delay element so as to match said time delay to a predetermined time period, and multiplier-summing circuit (18a-18n, 16a-16n and summing node) coupled to said delay element, for multiplying a signal output from said delay element and for summing said multiplied signal to generate and equalized signal.

Shirani shows each delay element (inductor and varactor diode) is calibrated by a respective control signal (60a). Shirani does not show means for selecting combinations of said lumped parameters to calibrate said delay element as called for in claims 8 and 18. Figure 2 of Yu et al. shows a delay line having a plurality of delay elements, each delay element is calibrated

by a selecting means (switches) to provide an accurate delay time and less sensitive to temperature fluctuation. Therefore, it would have been obvious to a person skilled in the art at the time of the invention was made to replace each of Shirani's varactor diode with a switch and a capacitor for the purpose of providing an accurate delay time that is less sensitive to temperature fluctuation.

Claims 21 and 22 are indefinite that the metes and bounds of the claim can not be determined thus, no prior art applied at this time.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P CALLAHAN can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan T. Lam
Primary Examiner
Art Unit 2816

11/29/2004